REMARKS

In an Office Action mailed on September 25, 2002, the Examiner made an objection to the drawings and maintained the § 103(a) rejections of claims 1-9 and 15-23 as being unpatentable over alleged Applicant's admitted prior art in view of Tjandrasuwita. For purposes of expediting prosecution, Figure 3, the figure objected to by the Examiner, as well as the corresponding text in the specification have been deleted for purposes of overcoming this objection. The specification has been amended accordingly to ensure correct references are made to the remaining figures. No new matter has been introduced. A copy of a Proposed Drawing Amendment that is being submitted concurrently herewith to change the figure numbers is enclosed. The original Proposed Drawing Amendment, showing the corrections in red ink, is being submitted concurrently herewith via first class mail. The § 103 rejections are discussed below.

Rejections of Claims 1-9:

Applicant requests the Examiner to consider all claim limitations. In this manner, claim 1 sets forth that the second circuit in a second mode, communicates indications of first data to an output terminal in synchronization with a first phase of a clock signal and prevents communication of second data during a second phase of the clock signal. The Examiner still fails to show where Tjandrasuwita teaches or suggests the above-recited claim limitations or where such limitations are disclosed by the alleged admitted prior art. Thus, for at least this reason, the Examiner fails to establish a *prima facie* case of obviousness for claim 1. Furthermore, in response to Applicant's contention that the Examiner has failed to provide support for the alleged suggestion or motivation to combine references, the Examiner still fails to provide a citation to any of the cited references that supports the alleged suggestion or motivation for the combination. Thus, for at least this additional reason, the Examiner fails to establish a *prima facie* case of obviousness for claim 1. Claims 2-9 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 10-14:

Similarly, the computer system of claim 10 specifies that the second circuit causes a first circuit to in a second mode, communicate indications of first data to a wire in synchronization

second phase of a clock signal. The Examiner fails to show this limitation in either alleged Applicant's admitted prior art or in Tjandrasuwita. Furthermore, the Examiner fails to provide support for a suggestion or motivation to combine Applicant's admitted prior art and Tjandrasuwita. Thus, for at least these reasons, withdrawal of the § 103 rejections of claims 10-14 is requested.

Rejections of claims 15-19:

The Examiner still fails to establish a *prima facie* case of obviousness for at least the reason that the Examiner fails to provide specific support for a suggestion or motivation to combine alleged Applicant's admitted prior art with Tjandrasuwita.

Thus, for at least this reason, a *prima facie* case of obviousness has not been established for claim 15, and withdrawal of the rejections of claims 15-19 is requested.

Rejections of Claims 20-23:

The method of claim 20 includes in a second mode, communicating first indications to a double pumped bus in synchronization with a first phase of a clock signal and preventing communication of the second indications to the double pumped bus during a second phase of the clock signal. The Examiner still fails to establish a *prima facie* case of obviousness for claim 20. In this manner, the Examiner provides no support for a suggestion or motivation to combine Tjandrasuwita with the alleged admitted prior art. Furthermore, Tjandrasuwita teaches disabling all communications, not disabling a data state associated with one phase of a clock signal and allowing communications to precede with another phase of a clock signal. Therefore, for at least this additional reason, the Examiner fails to establish a *prima facie* case of obviousness for claim 20.

Therefore, for at least these reasons, withdrawal of the § 103 rejections of claims 20-23 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the rejections of the claims and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0349US).

Respectfully submitted,

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Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

SPECIFICATION AMENDMENTS

The paragraph beginning on line 1 of page 3 has been rewritten as follows:

Referring to Fig. 2, several cells 12 and 14 (cells 14a, 14b and 14c, as examples) may be serially coupled together to from a chain to relay data between the cells 14 using the double pumped technique that is described above. In this manner, the cell 12 is the first in the chain, and the cells 14 precede the cell 12 in the chain. [As an example, Figs. 6, 7 and 8 depict signals called DP1, DP2 and DP3 that are furnished by the cells 12, 14a and 14b, respectively, and illustrate the propagation of data bits between the cells 12 and 14. For example, referring to Figs. 3, 4 and 5, the CLK signal (see Fig. 3) has a negative edge at time T_1, and in response to this negative edge, the cell 12 latches a bit (represented by the portion 50 of the DATA1 signal) for the first data set. At time T_2, the CLK signal has a positive edge, an edge that causes the cell 12 to latch a bit (represented by the portion 50 of the DATA2 signal) for the second data set. After time T_1 during the logic zero state of the CLK signal, the cell 12 begins furnishing the bit 50 to the cell 14a. It is noted that the bit 50 may not appear until after a slight propagation delay, as depicted in Fig. 5. After time T_2 during the logic one state of the CLK signal, the cell 12 begins furnishing the bit 52 to the cell 14a, as depicted in Fig. 6. The cells 14a and 14b then relay the bits 50 and 52 in a time multiplexed fashion as depicted in Figs. 7 and 8].

The paragraph beginning on line 27 of page 3 has been rewritten as follows:

Figs. 3 [4] and 5 [6] are schematic diagrams of double pumped bus cells according to embodiments of the invention.

The paragraph beginning on line 29 of page 3 has been rewritten as follows:

Fig. 4 [5] is a more detailed schematic diagram of the cell of Fig. 3 [4] according to an embodiment of the invention.

The paragraph beginning on line 1 of page 4 has been rewritten as follows:

Fig. 6 [7] is a schematic diagram of a double pumped bus cell system according to an embodiment of the invention.

The paragraph beginning on line 3 of page 4 has been rewritten as follows:

Fig. 7 [8] is a schematic diagram of a computer system according to an embodiment of the invention.

The paragraph beginning on line 7 of page 4 has been rewritten as follows:

Referring to Fig. 3 [4], an embodiment 100 of a double pumped bus cell in accordance with the invention may be set up to communicate either one or two sets of data. More specifically, in some embodiments of the invention, an EN signal that is received by the cell 100 may be asserted (driven high, for example) to enable the cell 100 to latch, store and retransmit bits of data from two different data sets in a time multiplexed fashion. In this manner, a data line 107 communicates a signal (called DATAIN) that indicates bits of data from a first data set and a second data set. The bits of the first data set are interleaved, or alternate, in time with the bits of the second data set.

The paragraph beginning on line 25 of page 5 has been rewritten as follows:

To accomplish the above-described features, in some embodiments of the invention, the cell 100 may include logic, such as an AND gate 112, that receives the CLK and EN signals. The output terminal of the AND gate 112 is coupled to the inverting clock input terminal of the bit latch 104, and the clock input terminal of the bit latch 102 [106] receives the CLK signal. Because the bit latches 102 and 104, in some embodiments of the invention, invert the logic levels of the stored bits, the cell 100 may include an inverter 108 that is coupled between the data input line 107 and the input terminals of the bit latches 102 and 104. When the EN signal is de-asserted, the output terminal of the AND gate 112 is de-asserted, regardless of the logic level of the CLK signal, and thus, the bit latch 104 does not store any new data as long as the EN signal remains de-asserted. However, when the EN signal is asserted, the CLK signal controls the signal at the output terminal of the AND gate 112 and thus, controls the reception of data into the bit latch 104.

The paragraph beginning on line 6 of page 6 has been rewritten as follows:

Fig. 4 [5] depicts a more detailed schematic diagram of the cell 100 in accordance with some embodiments of the invention. As shown, the bit latch 102 may include a circuit 140 that is effectively a complementary metal oxide semiconductor (CMOS) inverter that is enabled when

the CLK signal (that alternates between logic one and logic zero states) is in a logic one state to latch the bit that is indicated by the DATAIN signal. To accomplish this, the circuit 140 includes an n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) 148 that has its source terminal coupled to ground and its drain terminal coupled to the source terminal of another NMOSFET 146. The drain terminal of the NMOSFET 146 is coupled to the drain terminal of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) 144. The source terminal of the PMOSFET 144 is coupled to the drain terminal of another PMOSFET 142, and the drain terminal of the PMOSFET 142 is coupled to a positive voltage supply level (called V_{DD}). The gate terminals of the PMOSFET 144 and the NMOSFET 146 respond to the logical state of the CLK signal to control when the circuit 140 is enabled. In this manner, the gate terminal of the PMOSFET 144 is coupled to a clock input terminal 131 (that furnishes the CLK signal) via a chain 124 of three serially coupled inverters 240 that invert the CLK signal to receive an inverted version of the CLK signal. The gate terminal of the NMOSFET 146 is coupled to a chain 123 of serially coupled inverters 120 to the clock line 131 to receive an indication of the CLK signal. The gate terminals of the PMOSFET 142 and the NMOSFET 148 are coupled to the data input line 107.

The paragraph beginning on line 7 of page 8 has been rewritten as follows:

The cell 100 that is described above receives time-multiplexed bits of data from a single wire. However, in some embodiments of the invention, a cell 200 that is depicted in Fig. 5 [6] may be used in place of the cell 100. The cell 200 has a similar design to the cell 100 except for the following features. Unlike the cell 100, the cell 200 has two data input lines 203 and 205 (instead of one) to receive bits of data from circuits that are associated with two different data sets. In this manner, the inverter 108 (see Fig. 3 [4]) of the cell 100 is replaced by two inverters 202 and 207 of the circuit 200. The input terminal of the inverter 202 receives a signal (called DATA1) that is indicative of bits of data from the first data set, and the input terminal of the inverter 207 receives a signal (called DATA2) that is indicative of bits of data from the second data set. The output terminal of the inverter 202 is coupled to the data input line of the bit latch 102, and the output terminal of the inverter 207 is coupled to the data input line of the bit latch 104.

The paragraph beginning on line 19 of page 8 has been rewritten as follows:

Referring to Fig. 6 [7], in some embodiments of the invention, the cells 100 (the enabled cells 100a and the disabled cells 100b, as described below) and 200 may be used to form a double pumped bus chain 220 for purposes of communicating the bits of data from the first and second data sets across an integrated circuit, for example. In this manner, the cell 200 is the first in the chain 220 to arrange bits from the two different data sets in a time interleaved fashion. The cells 100 may be serially coupled together after the cell 200. As shown, to disable the flow of the bits of the data set that is associated with the DATA2 signal, every other cell 100 is disabled, as depicted in Fig. 6 [7] by the enabled cells 100a and the disabled cells 100b. This alternative disabling of the cells 100 occurs because each cell 100 reverses the phasing of the data flow. For example, each cell 100 receives the bits of a particular data set on positive clock edges and retransmits the bits of that data set on negative clock edges. The arrangement that is depicted in Fig. 6 [7] is used to disable the flow of bits for the data set that is associated with the DATA2 signal. However, alternatively, to disable the bits for the data set that is associated with the DATA1 signal, the enable input terminals 113 of the cells 200 and 100b are asserted, and the enable input terminals 113 of the cells 100a are de-asserted.

The paragraph beginning on line 4 of page 9 has been rewritten as follows:

Referring to Fig. 7 [8], as an example, the cell 200 (and/or the cell 100) may be used in a semiconductor circuit, such as a processor 252 (a microprocessor, such as a Pentium® microprocessor, as an example), to communicate bits of data between circuits 254, 256, 260 and 262 of the processor 252. In this manner, the cell 200 may communicate data over a wire 258 for two data sets. More specifically, the cell 200 may communicate data for a first data set between the circuit 254 that is located at one end of the wire 258 and the circuit 260 that is located at another end of the wire 268. The cell 200 may also communicate data for a second data set between the circuit 256 that is located at one end of the wire 258 and the circuit 262 that is located at the other end of the wire 268.